This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1 (Canceled)

2. (Original) A semiconductor device structure, comprising atop an FEOL semiconductor substrate:

a. a copper via level in electrical communication with the FEOL substrate and comprising also a solid permanent low-K dielectric material;

b. a gas impermeable etch stop level atop the permanent dielectric;

c. a permanent air dielectric level atop the etch stop;

d. a gas permeable hard mask atop the air dielectric level;

e. copper wiring having a top surface at the hard mask level and being in electrical communication with the via level; and

f. a thin protective cap on the top surface of the copper wiring.

3. (Original) A semiconductor device structure comprising a plurality of levels a-f recited in Claim 2.

4. (Original) The structure recited in Claim 3, wherein the solid permanent low-K dielectric material comprises a porous solid permanent low-K dielectric material.

5. (Original) The structure recited in Claim 3, wherein the solid permanent low-K dielectric material comprises a gas permeable solid permanent low-K dielectric material.

6. (Original) The structure recited in Claim 4, wherein the porous solid permanent low-K dielectric material is selected from the group consisting of porous SiLK, porous SiCOH and porous MSSQ.

7. (Original) The structure recited in Claim 5, wherein the gas permeable solid permanent low-K dielectric material is selected from the group consisting of SiLK, SiCOH, MSSQ, and JSR.

8. (Original) The structure in Claim 3, wherein between a minority of the total number of air dielectric levels and via level and via levels comprise also a strengthener.

9. (Canceled)

10. (Original) The structure recited in Claim 3, wherein the hard mask layer is selected from the group consisting of SiO_2, SiN, SiC, SiCH, and SiNCH.

11. (Original) The structure recited in Claim 10, wherein the hard mask layer is bi-layer, each layer of the bi-layer being selected from a different one of the group consisting of SiO_2, SiN, SiC, SiCH, and SiNCH.

12. (Original) The structure recited in Claim 3, wherein the cap is selected from the group consisting of CoWP, Ta, W, TaN, Ru and any combination thereof.

13. (Original) An initial subset for a semiconductor device structure, comprising atop an FEOL semiconductor substrate:

a. a gas impermeable etch stop level atop the substrate;

b. a first copper line level in electrical communication with the FEOL substrate, the first line level also comprising a permanent air dielectric material atop the etch stop;

c. a first copper via level atop and in electrical communication with the first copper line level, the first via level also comprising a first permanent porous ultra-low dielectric material;

d. a second copper line level in electrical communication with the first via level, the second line level also comprising a sacrificial material which is subject to decomposition and removal under process heating; and

e. atop the second line level, a layer of permanent ultra-low dielectric material which is subject to forming porosities under process heating.

14. (Original) The structure recited in claim 13, wherein the permanent ultra-low dielectric material which is subject to forming porosities under process hearing is selected from the group consisting of porous SiLK, porous SiCOH and porous MSSQ.

15. (Original) The structure recited in claim 13, wherein the sacrificial material which is subject to decomposition and removal under process heating is selected from the group consisting of polystyrenes; polymethyl methacrylates; polynorbornenes; and polypropylene glycols

16. (Canceled)

17. (Original) The structure recited in claim 13, comprising also a hard mask layer between line level and via level.

18. (Original) The structure recited in Claim 17, wherein the hard mask layer is selected from the group consisting of SiO_2, SiN, SiC, SiCH and SiNCH.

19. (Withdrawn) A process for fabricating a semiconductor device structure atop an FEOL semiconductor substrate, comprising:

a. depositing a first layer of permanent ultra-low K dielectric material atop the substrate, in which layer will be fabricated the first via level.

b. depositing a first layer of sacrificial material atop the first layer of permanent dielectric material, in which layer will be fabricated the first line level;

c. fabricating the first copper via and line levels by dual damascene processing and planarizing the first hard mask to expose the surface of the copper lines;

d. selectively depositing a thin protective cap on the exposed copper lines;

e. applying a blanket of permanent dielectric atop the wiring level; and

f. annealing the structure under vacuum in an inert atmosphere by gradually increasing the temperature to a level and for a time sufficient to decompose and remove the sacrificial material.

20. (Withdrawn) The process recited in claim 19, including the step of applying a first gas impermeable etch stop layer between the first permanent ultra-low K dielectric material and the first sacrificial layer.

21. (Withdrawn) The process recited in claim 20, wherein the step of applying a first gas impermeable etch stop comprises applying a first gas impermeable etch stop selected from the group consisting of SiO_2, SiN, SiC, SiCH, and SiNCH.

22. (Withdrawn) The process recited in claim 19, wherein the first layer of permanent ultra-low K dielectric material is selected from the group consisting of SiLK and porous SiLK, JSR, MSSQ and porous MSSQ.

23. (Withdrawn) The process recited in claim 19, wherein the first layer of sacrificial material is selected from the group consisting of polystyrenes; polymethyl methacrylates; polynorbornenes; and polypropylene glycols.

24. (Withdrawn) The process recited in claim 19, wherein the first gas permeable hard mask is selected from the group consisting of HOSP and HOSP Best, JSR 5140, JSR 2021, SiCOH, polycarbonates and any combination thereof.

25. (Withdrawn) The process recited in claim 19, wherein the cap is selected from the group consisting of CoWP, Ta, W, TaN, Ru, and any combination thereof.

26. (Withdrawn) The process recited in claim 19, wherein the steps of a-g are repeated atop the annealed structure at step g as substrate until attaining the number of levels desired.

27. (Withdrawn) Fabricating an initial subset for a semiconductor device structure, comprising atop an FEOL semiconductor substrate:

a. providing a gas impermeable etch step level atop the substrate;

b. depositing a first sacrificial dielectric material atop the etch stop and a first permeable CMP hard mask atop the first sacrificial dielectric;

c. fabricating an opening through the hard mask and depositing therein a first copper line level for electrical communication with the FEOL substrate;

d. planarizing to expose the copper lines and make them even with the first hard mask, and applying thereover a first permanent, solid, partially cured ultra-low K dielectric material which is capable of developing porosities at processing temperature;

e. providing a first anneal to the structure under vacuum in an inert atmosphere by gradually increasing the temperature to a level and for a time sufficient to decompose and

remove the sacrificial material from the first line level while also finally curing and creating porosities in the permanent ultra-low K dielectric material;

f. applying a second layer of sacrificial dielectric atop the first permanent ultra-low K dielectric material, and applying a second permeable hard mask thereover;

g. fabricating the first copper via and second copper line levels on the second hard mask by dual damascene processing and planarizing to expose the surface of the copper lines and make them even with the second permeable hard mask.

h. applying on the second permeable hard mask a second permanent, solid, partially cured ultra-low K dielectric material which is capable of developing porosities at processing temperature; and

i. providing a second anneal to the structure under vacuum in an inert atmosphere by gradually increasing the temperature to a level and for a time sufficient to decompose and remove the sacrificial material from the second line level while also finally curing and creating porosities in the second permanent ultra-low K dielectric material.

28. (Withdrawn) The process recited in claim 27, wherein steps g-I are repeated as required.

29. (Withdrawn) The process recited in claim 28, wherein the steps of applying permanent, solid, partially cured ultra-low K dielectric material which is capable of developing porosities at processing temperature comprises applying a material selected from the group consisting of SiLK, MSSQ, and SiCOH.